IN THE SPECIFICATION:

Please amend the paragraph that begins at page 9, line 2, as follows:

When the test mode signal TEST indicates the test mode, the multiplexer 13 accordingly outputs predetermined read data (fourth read data RD3 in the present embodiment) in the first to fourth read data RD0 to RD3. In the test mode, the CPU 11 receives the fourth read data RD3 and compares the fourth read data RD3 with write data that has been written previously in the fourth memory circuit RAM3. Based on the comparison result, the CPU 11 checks if the write data written in the fourth memory circuit RAM3 has been read accurately, and supplies a confirmation signal K1 indicating the comparison result to an external apparatus ~~(not shown)~~ 100 via the input/output circuit 15.

Please amend the paragraph that begins at page 9, line 14, as follows:

The comparator 14 receives the first to fourth read data RD0 to RD3, compares the first to fourth read data RD0 to RD3 with one another and supplies the external apparatus (testing apparatus~~, not shown~~) 100 with a decision signal K2 indicating if all of the read data RD0 to RD3 match with one another.

Please amend the paragraph that begins at page 18, line 11, as follows:

The comparator 72 includes a register (not shown) for storing the results of comparing all of the read data RD0 to RD3 with one another. The CPU 71 receives comparison results stored in the register of the comparator 72 and provides a signal indicating whether the first to fourth memory circuits RAM0 to RAM3 are operating

normally. The signal is supplied to an external apparatus ~~(not shown)~~ 100 via the input/output circuit 15 based on the comparison results and the results of comparing whether the read data from the memory circuits coincide with the write data. As the CPU 71 outputs the test results, the testing apparatus ~~(not shown)~~ 100 only has to receive the test results from the semiconductor device 70. This simplifies the structure of the testing apparatus. The testing apparatus can acquire test results regardless of the operational speed of the semiconductor device 70.

Please amend the paragraph that begins at page 19, line 24, as follows:

For example, the comparator 81 outputs an L-level signal as a result of the reset operation, and latches an H-level signal when the read data from the first to fourth memory circuits RAM0 to RAM3 do not coincide with one another. A decision signal K2a or the output signal of the comparator 81 is supplied to a testing apparatus ~~(not shown)~~ 200 coupled to the semiconductor device 80, and the testing apparatus determines whether the semiconductor device 80 is defective in accordance with the decision signal K2a. In this case, since the decision signal K2a is latched by the comparator 81, even a testing apparatus, which operates according to a clock slower than the operational clock of the semiconductor device 80, can reliably receive the decision signal K2a. Even if the operational speed of the semiconductor device becomes faster, therefore, a memory test on the semiconductor device can be conducted without replacing the testing apparatus with one that matches the operational speed. This prevents the test cost from increasing. Further, the memory test can be

carried out while operating the semiconductor device 80 at actual operational speed of the semiconductor device, regardless of the operational speed of the testing apparatus. This makes it possible to accurately determine whether the memory circuits RAM0 to RAM3 are failing.